

**UTILITY PATENT APPLICATION TRANSMITTAL  
(Large Entity)***(Only for new nonprovisional applications under 37 CFR 1.53(b))*Docket No.  
Q00-1041-US1

Total Pages in this Submission

**TO THE ASSISTANT COMMISSIONER FOR PATENTS**Box Patent Application  
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

**Mixed Signal Adaptive Boost Equalization Apparatus and Method**

and invented by:

**Andrew Bishop, Ivan Chan, and Russell W. Brown**If a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information:☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: \_\_\_\_\_

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Enclosed are:

**Application Elements**

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 16 pages and including the following:
  - a. ☒ Descriptive Title of the Invention
  - b. ☐ Cross References to Related Applications *(if applicable)*
  - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
  - d. ☐ Reference to Microfiche Appendix *(if applicable)*
  - e. ☒ Background of the Invention
  - f. ☐ Brief Summary of the Invention
  - g. ☒ Brief Description of the Drawings *(if drawings filed)*
  - h. ☒ Detailed Description
  - i. ☒ Claim(s) as Classified Below
  - j. ☒ Abstract of the Disclosure

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**Application Elements (Continued)**

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
- a. ☒ Formal                      Number of Sheets 8
- b. ☐ Informal                      Number of Sheets \_\_\_\_\_
4. ☒ Oath or Declaration
- a. ☒ Newly executed *(original or copy)*                      ☐ Unexecuted
- b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
- c. ☒ With Power of Attorney                      ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)  
Signed statement attached deleting inventor(s) named in the prior application,  
see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*  
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under  
Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby  
incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy *(identical to computer copy)*
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

**Accompanying Application Parts**

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449                      ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
- ☐ First Class    ☒ Express Mail *(Specify Label No.):* EL111015817US

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**Accompanying Application Parts (Continued)**

15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)

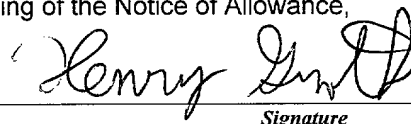
16. ☐ Additional Enclosures (please identify below):

**Fee Calculation and Transmittal**

**CLAIMS AS FILED**

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	11	- 20 =	0	x \$18.00	\$0.00
Indep. Claims	2	- 3 =	0	x \$78.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$690.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$690.00

- ☐ A check in the amount of \_\_\_\_\_ to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 50-0283 as described below. A duplicate copy of this sheet is enclosed.
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Signature

Henry Groth, 39,696  
Quantum Corporation, Patent Department, Building 6  
500 McCarthy Boulevard, Milpitas, CA 95035  
voice 408-894-5425, fax 408-232-6581  
email henry.groth@quantum.com

Dated: 8/28/2000

CC:

## **MIXED SIGNAL ADAPTIVE BOOST EQUALIZATION APPARATUS AND METHOD**

### **BACKGROUND OF THE INVENTION**

#### **1. Field of the Invention**

The present invention generally relates to high-speed binary communications. More specifically, the invention relates to a novel apparatus and method which reduces Inter-Symbol Interference (ISI) under variable cabling environments within the SCSI protocol.

#### **2. Description of Related Art**

Computers are generally constructed with at least one parallel data bus capable of transferring digital information between a host computer processor and hardware devices such as printers, scanners, disk drives, etc. FIG. 1 illustrates a parallel bus 100 connected to a host 120 and various hardware devices 140a... 140m. The number of hardware devices 140a... 140m that can communicate via parallel bus 100 is limited by the type of electronic interface, i.e., bus, used in the computer's design.

One well-known electronic interface that is employed in the architecture of computers is the Small Computer System Interface (SCSI). SCSI is a set of ever changing electronic interface standards that allow faster and more flexible parallel communication between computers and peripheral hardware over previous interfaces. The maximum length of cable that can comprise the bus as well as the maximum number of devices that can be connected to it is dictated by the specific SCSI standard employed within the computer. For example, the SCSI-1 standard specifies a bus that can be six meters in length and can interconnect up to eight devices.

A list of the currently adopted SCSI standards and their main attributes are summarized in TABLE 1.

TABLE 1

SCSI Standard	Maximum Cable Length (m)	Maximum Speed (Mbytes/sec)	Maximum Number of Devices
SCSI-1	6	5	8
SCSI-2	6	5-10	8 or 16
Fast SCSI-2	3	10-20	8
Wide SCSI-2	3	20	16
Fast Wide SCSI-2	3	20	16
Ultra SCSI-3, 8-bit	1.5	20	8
Ultra SCSI-3, 16-bit	1.5	40	16
Ultra-2 SCSI	12	40	8
Wide Ultra-2 SCSI	12	80	16
Ultra-3 (Ultra160/m) SCSI	12	160	16

SCSI interfaces are susceptible to the same signal distortion interference that is seen in most digital transmission devices. As data transmission speeds and cable lengths increase, signals transmitted using SCSI interfaces become vulnerable to inter-symbol interference (ISI), which, in a digital transmission system, is distortion of the received signal. This distortion is exhibited by temporal spreading and consequent overlap of individual pulses to the degree that the receiver cannot reliably distinguish between change of states, i.e., between individual signal elements.

Contributing factors leading to inter-symbol interference include timing inaccuracies between pulse timing and the channel ringing; insufficient bandwidth; amplitude distortion as a function of frequency; phase distortion as a function of frequency; variations in loading conditions as a function of the number of devices connected to the cable; and length of the cable.

Regardless of the circumstances responsible, inter-symbol interference results in unreliable data detection when messages are passed between two or more devices in a SCSI environment. In an effort to combat the effects of ISI, several conventional equalization approaches have been adopted. In one approach, equalization of the digital pulse signal is accomplished by utilizing a second order zero ( $s^2$ ) in the frequency domain to narrow the pulse into a pre-defined target shape. Maximum likelihood detectors are then used to extract the relevant data. This approach reduces the amplitude distortion effect associated with ISI, but is practically useless against correcting phase distortion.

Another conventional approach employs a matched filter having a transfer function that is the inverse of the transmission media transfer function. This approach acts to neutralize both the amplitude and phase distortion induced by the cable. While this is an effective method for the reduction of ISI, it is impractical because of the multiple signal lines that are utilized with the SCSI communication link. In addition, the SCSI cabling environment must accommodate a wide variety of device configurations making this scheme difficult as well as economically infeasible to provide a single match filter that encompasses all cases.

An apparatus and method is needed, therefore, that can overcome the limitations of conventional approaches, thereby reducing ISI in a variable cable environment and making data detection reliable. Additionally, a need exists such that the implementation of the apparatus and method is relatively easy and cost effective.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a high-level functional block diagram of a host coupled to various hardware devices via a parallel bus and equalization apparatuses.

FIG. 2 is a high-level functional block diagram depicting a more specific embodiment of the equalization apparatuses.

FIG. 3 is a functional block diagram illustrating an implementation of an adaptive filter element.

FIG. 4 is a functional block diagram that illustrates the circuit used for comparison of a training waveform to a threshold level. In addition, adjustment of the threshold level is depicted.

FIG. 5 is a high-level functional block diagram depicting an embodiment of filter adaptation circuitry.

FIG. 6 illustrates the magnitude frequency response of a typical filter with and without a high frequency gain boost.

FIG. 7 illustrates the relationship of signals used for filter adaptation to an input waveform and the results these have on the boost gain.

FIG. 8 depicts the transient response of an unequalized signal and an adaptively equalized signal.

## DETAILED DESCRIPTION

The following detailed description refers to the accompanying drawings that illustrate embodiments of the present invention. Other embodiments are possible and modifications may be made to the embodiments without departing from the spirit and scope of the invention. Therefore, the following detailed description is not meant to limit the invention. Rather, the scope of the invention is defined by the appended claims.

Furthermore, it will be apparent to one of ordinary skill in the art that the embodiments as described below may be implemented in many different embodiments of software, firmware, and hardware in the entities illustrated in the figures. The actual software code or specialized control hardware used to implement the present invention is not limiting of the present invention. Hence, the operation and behavior of the embodiments will be described without specific reference to the actual software code or specialized hardware components. It is understood that artisans of ordinary skill would be able to design software and control hardware to implement the embodiments of the present invention based on the description herein.

FIG. 1 shows an overall block diagram of one embodiment of the invention. A host 120 and various hardware devices 140a... 140m are coupled to parallel bus 100 via channel interfaces 105a... 105m, respectively. The host 120 can be any of a wide variety of central processor units, i.e., Intel Processors, AMD Processors, and the like. Hardware devices 140a... 140m include CD ROM record/playback devices, disk drives, scanners, printers, or any other peripheral device designed for communication via parallel bus 100. Channel interfaces 105a... 105m facilitate the connection of the individual devices, e.g., host 120 and hardware devices 140a... 140m, to the respective lines of parallel bus 100 from whence information, e.g., digital data in the form of an oscillating signal over each line, is received.



Equalization apparatuses 110a... 110m reduce the effects of inter-symbol interference (ISI) that is introduced into an oscillating signal as a consequence of various factors including the distance that a signal has to travel on parallel bus 100, the characteristics of the cable that comprises parallel bus 100, and the number of devices coupled to parallel bus 100. Each equalization apparatus has two modes of operation, a training mode and a normal mode.

FIG. 2 depicts a more detailed representation of an embodiment of the present invention. This high-level block diagram illustrates the functionality of adaptive ISI equalization apparatuses 110a... 110m. Each equalization apparatus 110a... 110m consists of an adaptive filter element 210, comparator component 220, digital-to-analog converters (DACs) 250 and 260, threshold adjust circuitry 240, filter adaptation circuitry 230, and an adder circuit 245. Switches 235 and 236, shown in the normal mode of operation, are not physically embedded within equalization apparatuses 110a... 110m. Rather, they are used for illustrative purposes to aid in the discussion of operation of the invention, as presented below.

In the normal mode of operation, the adaptive filter element 210 receives signals (e.g., input signal 200) transmitted by the host device and outputs signals within a specified frequency range. An externally controlled adjustable gain is incorporated into adaptive filter element 210 for tuning the filter to a predetermined frequency band. The characteristics of adaptive filter element 210 are such that only the high-end frequency components of the received signal within this predetermined frequency band are adjusted. These adjustments are made to the higher frequency components of the received signals because they are more susceptible to ISI effects than lower frequency signals.

Adaptive filter element 210 is characterized by the transfer function,  $(Ks + a)/D(s)$ , where the “Ks” term in the numerator indicates a first order boost with a gain of K. In this

implementation, equalization of the received signal is accomplished by adaptive filter element 210 via adjustable gain, K. Such adjustment is controlled by filter adaptation circuitry 230. The magnitude frequency response of a typical filter, with and without a high frequency boost gain, is shown in FIG. 6.

An embodiment of adaptive filter element 210 utilized by the ISI adaptive equalizer apparatuses 110a... 110m is shown in FIG. 3. The filter element 210 is configured as a 3<sup>rd</sup> order Bessel filter with functional components including a multiplicity of transconductance amplifiers 300, 302, ... 310 with gain gm, and a multiplicity of capacitors C1 320, C2 330, and C3 340. In this embodiment, the input signal  $V_{in}$  380 is applied to transconductance amplifier 300. The voltage on C2 330 provides the 1<sup>st</sup> order term and is amplified by adjustable amplifier 350 with variable gain K. The voltages on capacitors C2 330 and C3 340 are added together to produce the output,  $V_{out}$  370, of the adaptive filter element 210. Output  $V_{out}$  370 can be expressed as:

$$V_{out} = K * V2 + V3$$

where V2 and V3 are the voltages on capacitors C2 330 and C3 340, respectively, and K is a value between 0 and 2.

The magnitude of the gain parameter, gm, of transconductance amplifiers 300, 302, ...310 controls the bandwidth of the filter and capacitance values C1 320, C2 330, and C3 340 control the location of the filter's poles. Component values of adaptive filter element 210 that provide exceptional response include C1 = 0.265pF, C2 = 0.764pF, C3 = 1.326pF, and gm = 800  $\mu$ A/V.

The preceding discussion focused on the normal mode of operation of equalization apparatuses 110a... 110m. Operation of apparatuses 110a... 110m in the training mode is accomplished by coupling switches 235 and 236 of FIG. 2 to the threshold adjust circuitry 240

and filter adaptation circuitry 230, respectively. This mode of operation uses a known waveform, i.e., training signal, to calibrate the adaptive filter before pertinent data is sent from host 120 to hardware devices 140a... 140m, thereby minimizing ISI effects and allowing for the reliable detection of transmitted information. The training pattern may comprise a pulse train of alternating 1's and 0's, e.g., 1010..., or may be a more complex pseudo-random bit pattern. The waveform used for training each equalization apparatus 110a... 110m is inconsequential, provided each apparatus knows a priori the bit pattern corresponding to the training waveform used for calibration.

During the training mode of operation, before calibration of adaptive filter element 210 can be accomplished, detection of whether or not the training signal is above or below a certain threshold level must be ascertained. FIG. 4 shows a block diagram consisting of a threshold adjust circuit 240 and the components used for signal detection. The output of adaptive filter 210,  $V_{out}$  370, is applied to the inverting input of comparator 220, where it is compared with a threshold value. Comparator 220 outputs a digital logic low if  $V_{out}$  370 is above the threshold value and a digital logic high if  $V_{out}$  370 is below the threshold value. The logic value outputted from comparator 220 is sensed at the input of D flip-flop 400 and is subsequently captured with the rising edge of the synchronous reference clock (CLK) 435. The outputs of D flip-flop 400, Below 455 and Belownot 456, are then used by filter adaptation circuitry 230 to adjust the boost gain, K, of adaptive filter element 210.

The threshold value is set by threshold adjust circuit 240 at the beginning of the pulse train that comprises the signal used in the training mode of operation. A DC level corresponding to the highest negative peak amplitude a data signal can obtain is transmitted by host 120 to equalization apparatuses 110a... 110m. The threshold value is then fine tuned via adder circuitry

245 until a transition in the output of comparator 220 is sensed, at which time threshold adjustment ceases. All subsequent transmissions from host 120 are compared against this threshold value. It should be noted that in a related embodiment of the invention, a DC level corresponding to the highest positive peak could just as well have been used with a reversal in comparator 220 inputs and a positive threshold value.

A high-level schematic of filter adaptation circuitry 230 is shown in FIG. 5. Once the threshold level has been set by threshold adjust circuitry 240, filter adaptation is accomplished using the waveform of training pattern 525. As noted earlier, the data bit pattern corresponding to the training waveform as to when in time transitions occur must be known by equalization apparatuses 110a... 110m before filter adaptation takes place. As depicted in FIG. 5, training pattern 525 is captured by D flip-flop 500 and subsequently by D flip-flop 510 using CLK 435. D flip-flops 500 and 510 are used in conjunction with AND gate 550 to detect a falling edge in the training waveform. The output signal, Falling Edge 575, of AND gate 550, is inputted into AND gates 560 and 570 along with logic signals Below 455 and Belownot 456, with Below 455 being input to AND gate 560 and Belownot 456 being input to AND gate 570, to generate logic signals errBelow 565 and noerrBelow 566. The signals errBelow 565 and noerrBelow 566 are subsequently captured by D flip-flops 530 and 540, respectively, and are then used as select lines for multiplexer (MUX) 580. The logic levels of errBelow 565 and noerrBelow 566 determine whether or not the boost gain, K, of adaptive filter element 210, should be increased or decreased. In this embodiment of the invention, if errBelow 565 is logic high and noerrBelow 566 is logic low, K will be increased by a programmable value, u, which controls the rate of adaptation. If, on the other hand, noerrBelow 566 is logic high and errBelow 565 is logic low, then K will be decreased by the amount u. If the signals, 565 and 566, are either high or low

simultaneously, then the boost gain,  $K$ , remains constant. In this way, the boost gain,  $K$ , of adaptive filter element 210 is adjusted so that the amplitude of the filtered high frequency signal matches the negative DC reference voltage. The M-bit coefficient register 590 and N-bit coefficient register 515 are used to store and program the boost signal gain,  $K$ . FIG. 7 illustrates with a timing diagram the relationship of the signals, generated in FIGS. 4 and 5, to the input waveform as well as the result on the boost signal gain,  $K$ .

FIG. 8 shows the transient response of an unequalized signal, e.g., Input Signal 200, (top waveform) and an adaptively equalized signal, e.g., Output Signal 270, (bottom waveform) as processed by the present invention. As stated previously, two modes of operation are employed by equalization apparatuses 110a... 110m. Each apparatus 110a... 110m is in training mode between 0 and 500ns. Between 0 and 50ns, the host asserts a DC voltage level of  $-200$  mV in order to set the threshold level; between 50ns and 500ns, the host device transmits the high frequency training pattern '101010...'; and after 500ns the equalization apparatuses 110a... 110m are placed in the normal mode of operation and digital information-bearing signals are transmitted by host 120. It is to be noted that adaptive equalization is accomplished during the first 300ns of the training pattern.

Referring to the unequalized signal, it can be seen that the negative peak amplitude of the high frequency transmission signal is approximately  $-100$  mV or half of the asserted DC voltage level. During the transmission of data signals, amplitudes of consecutive negative and positive peaks can vary by as much as 100 mV.

For the equalized signal beyond  $\sim 160$ ns, the negative peak amplitude of the high frequency transmission signal is boosted so that it consistently approximates the threshold level that was determined at the beginning of the training pulse, i.e., the DC voltage level of  $-200$  mV.

The subsequent information-bearing signals are equalized in the manner explained previously, as is depicted by the output (equalized) signal in FIG. 8.

Thus, by equalizing the high frequency components, the amplitudes of the information-bearing signals become relatively constant and ISI effects are minimized. The success of adaptive equalization apparatuses 110a... 110m make them attractive for use in high-speed data transfer variable SCSI cabling environments.

It is important to note that the foregoing description of embodiments of the present invention provides illustration and description, but is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications and variations are possible consistent with the above teachings or may be acquired from practice of the invention. The claims and their equivalents define the scope of the invention.

**WHAT IS CLAIMED:**

1. A circuit for adaptively amplifying an input signal, the circuit comprising:  
an adaptive filter connected to receive the input signal and to amplify a predetermined frequency range of the input signal by an amount based on an amplification control signal input to the adaptive filter;

a comparator connected to receive the amplified signal from the adaptive filter and a predetermined threshold signal, the comparator outputting a digital comparison signal indicating whether the amplified signal is greater than the threshold signal; and

a filter adaptation circuit connected to receive the digital signal and the input signal and to modify the amplification control signal based on the digital signal and the input signal.

2. The circuit of claim 1, wherein the input signal is a SCSI (small computer system interface) signal and the adaptive filter reduces inter-symbol interference (ISI) in the SCSI signal.

3. The circuit of claim 1, wherein the predetermined frequency range amplified by the adaptive filter consists of high frequency components of the input signal.

4. The circuit of claim 1, wherein the adaptive filter is a third order Bessel filter.

5. The circuit of claim 1, further comprising  
a digital-to-analog converter converted connected between the adaptive filter and the filter adaptation circuit, the digital-to-analog converter converting a digital version of the

Parameter	Value	Unit
Temperature	25	°C
Pressure	1	atm
Concentration	0.1	M
Time	10	min
Volume	100	μL
Flow rate	1	μL/min
Wavelength	254	nm
Scan rate	10	nm/min
Resolution	0.1	nm
Integration time	1	s
Repetition rate	10	Hz
Beam diameter	1	mm
Spot size	100	μm
Field of view	1000	μm
Pixel size	10	μm
Sampling rate	10	Hz
Integration time	1	s
Repetition rate	10	Hz
Beam diameter	1	mm
Spot size	100	μm
Field of view	1000	μm
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Sampling rate	10	Hz
Integration time	1	s
Repetition rate	10	Hz
Beam diameter	1	mm
Spot size	100	μm



6. The circuit of claim 5, wherein the filter adaptation circuit further comprises:

a first circuit connected to receive the digital signal, the input signal, and a system clock signal, the first circuit converting the digital signal, the input signal, and the system clock signal into a first output signal that is asserted on a falling edge of a digitized version of the input signal when the input signal is above a level of the predetermined threshold signal and a second output signal that is asserted on the falling edge of the digitized version of the input signal when the input signal is below the level of the predetermined threshold signal; and

a second circuit connected to receive the first and second output signals and to increase the amplification control signal when the first signal is asserted and the second signal is not asserted and to decrease the amplification control signal when the first signal is not asserted and the second signal is asserted.

7. A method of canceling inter-symbol interference (ISI) in a SCSI (small computer system interface) signal, the method comprising:

amplifying high frequency components of an input SCSI signal by an amount based on an amplification control signal;

comparing the amplified signal with a predetermined threshold level; and

iteratively modifying the amplification control signal based on a result of the comparison of the amplified signal with the predetermined threshold level.

8. The method of claim 7, wherein modifying the amplitude control signal includes:

increasing the amplitude control signal on a falling edge of a digitized version of the input signal when the input signal is above the predetermined threshold level and decreasing the amplitude control signal on the falling edge of the digitized version of the input signal when the input signal is below the predetermined threshold level.

9. The method of claim 7, wherein the threshold level is a voltage offset from the voltage level used to covert the input SCSI signal to a digital value.

10. The method of claim 9, wherein the threshold voltage level is below the voltage level used to convert the input SCSI signal to a digital value.

11. The method of claim 7, wherein the amplification of the high frequency components is performed using a third order Bessel filter.

The high frequency components of a SCSI signal are adaptively equalized using an adaptive filter having an adjustable gain. A comparator is used to compare an input signal with a predetermined threshold level. Based on the result of the comparison, the adjustable gain of the adaptive filter is modified.

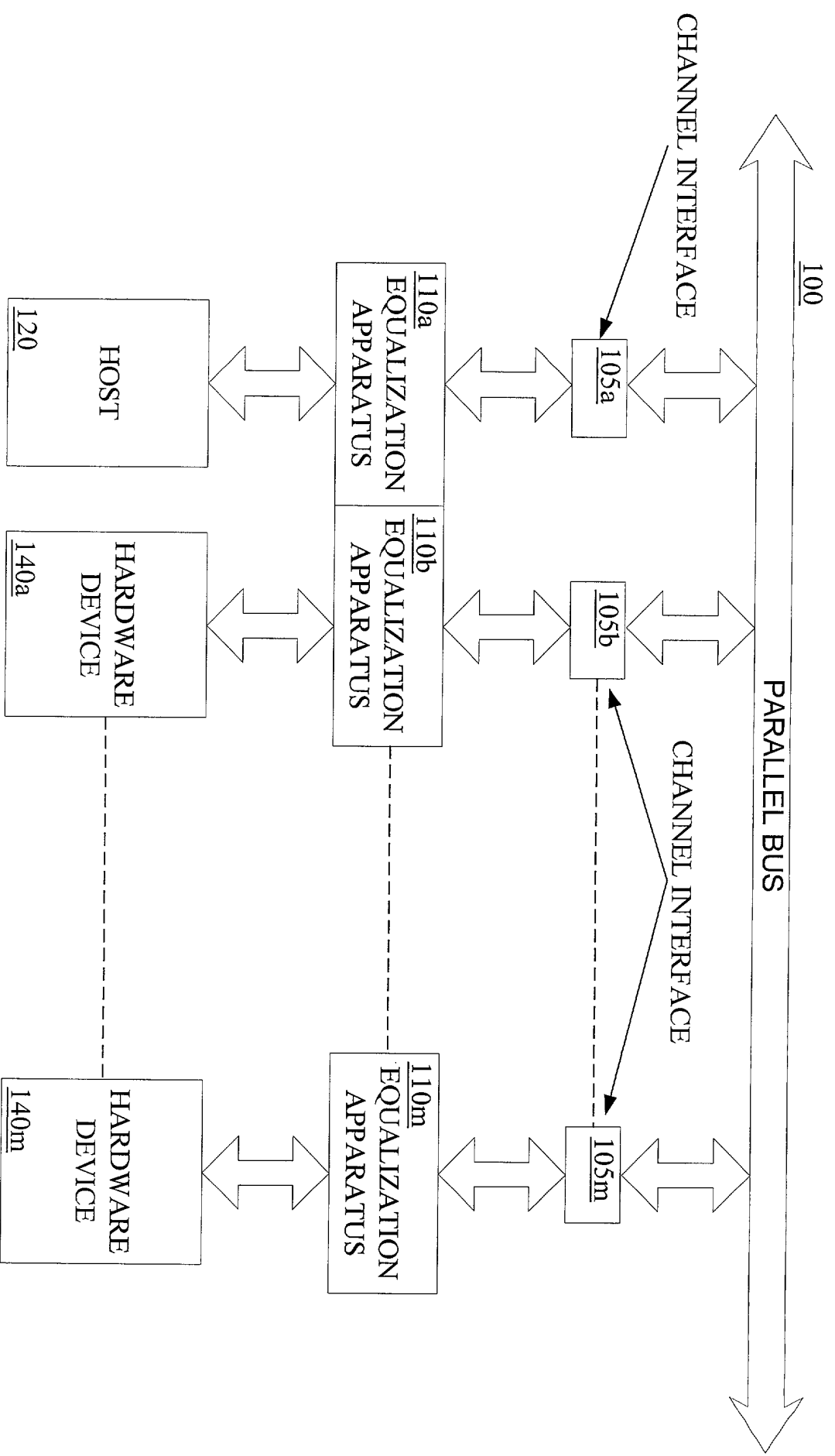
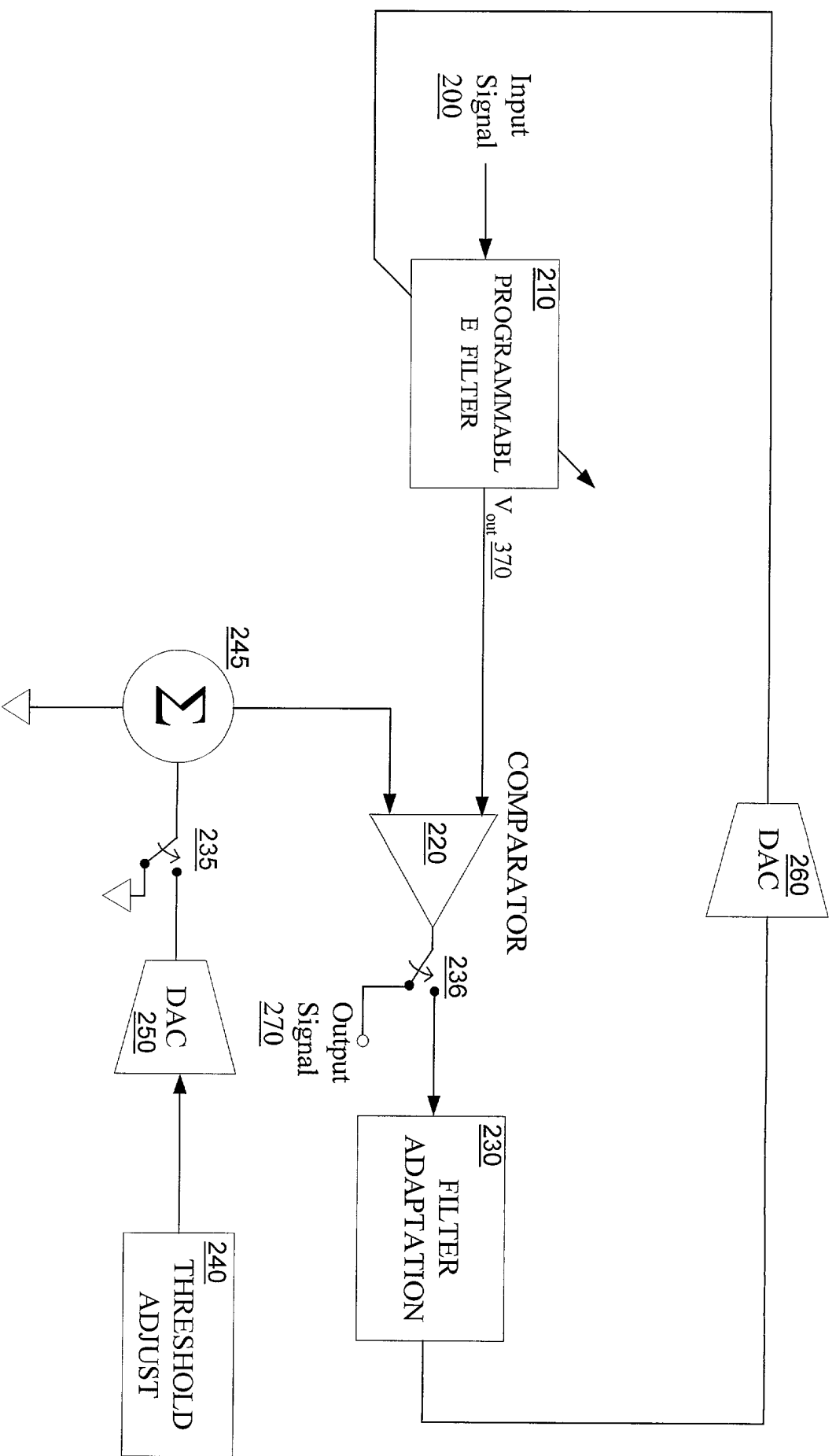


FIG. 1

FIG. 1 is a block diagram of a parallel bus system with equalization apparatuses and hardware devices.



110a... 110m

FIG. 2



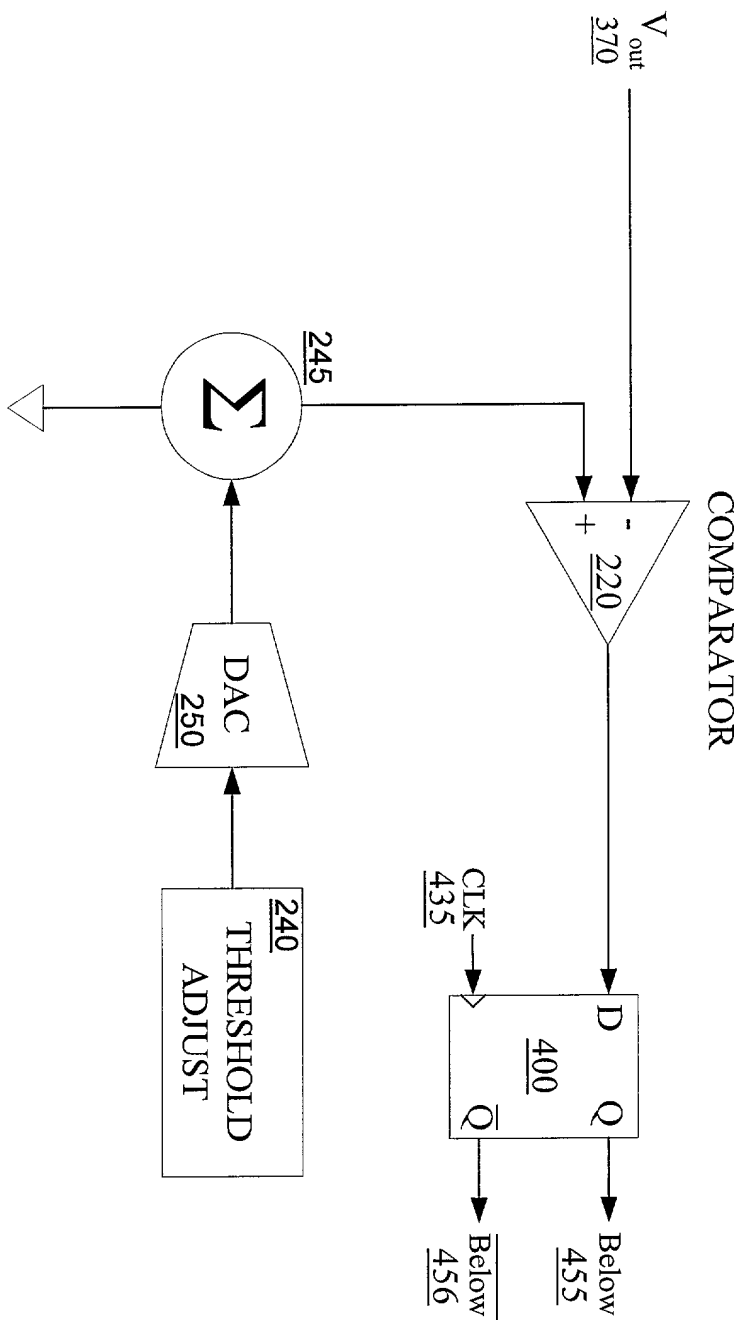
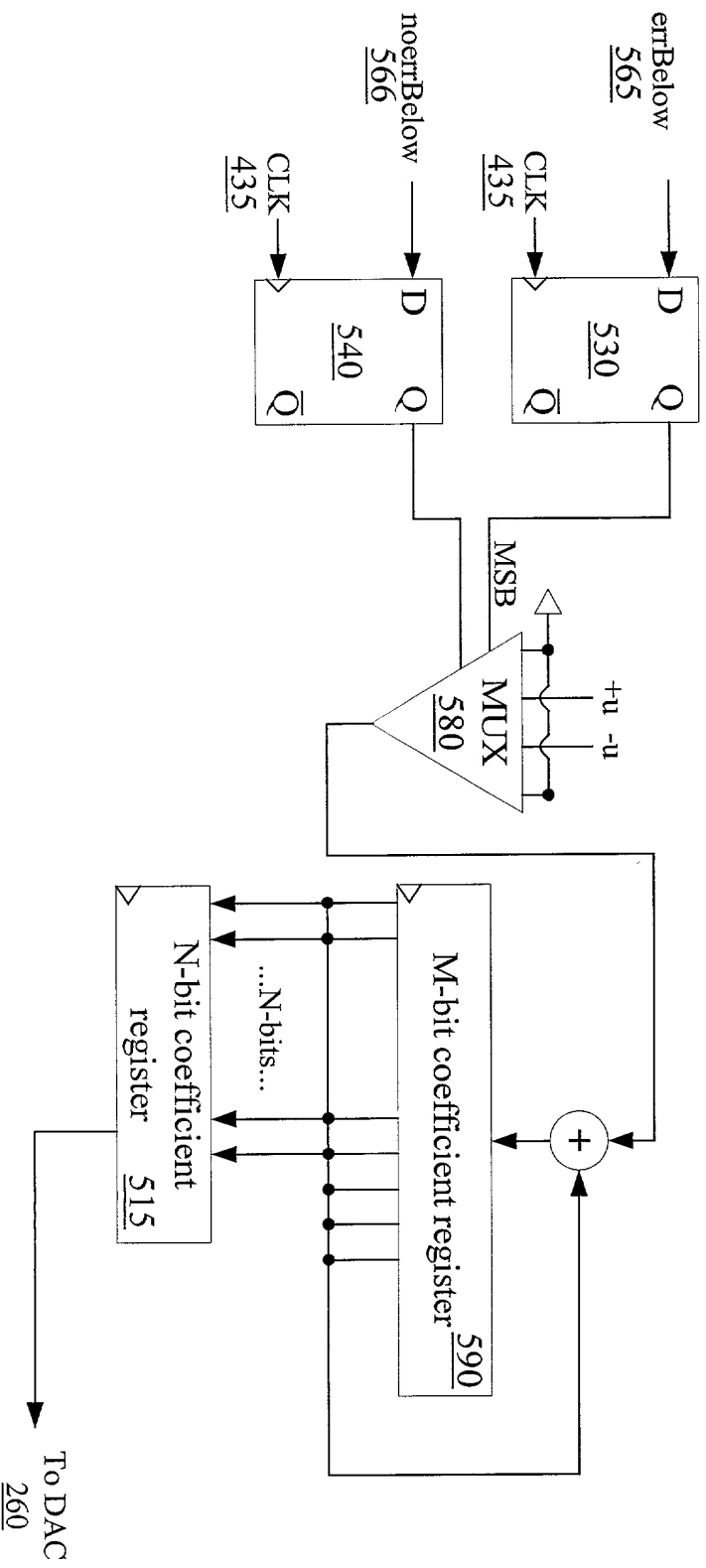
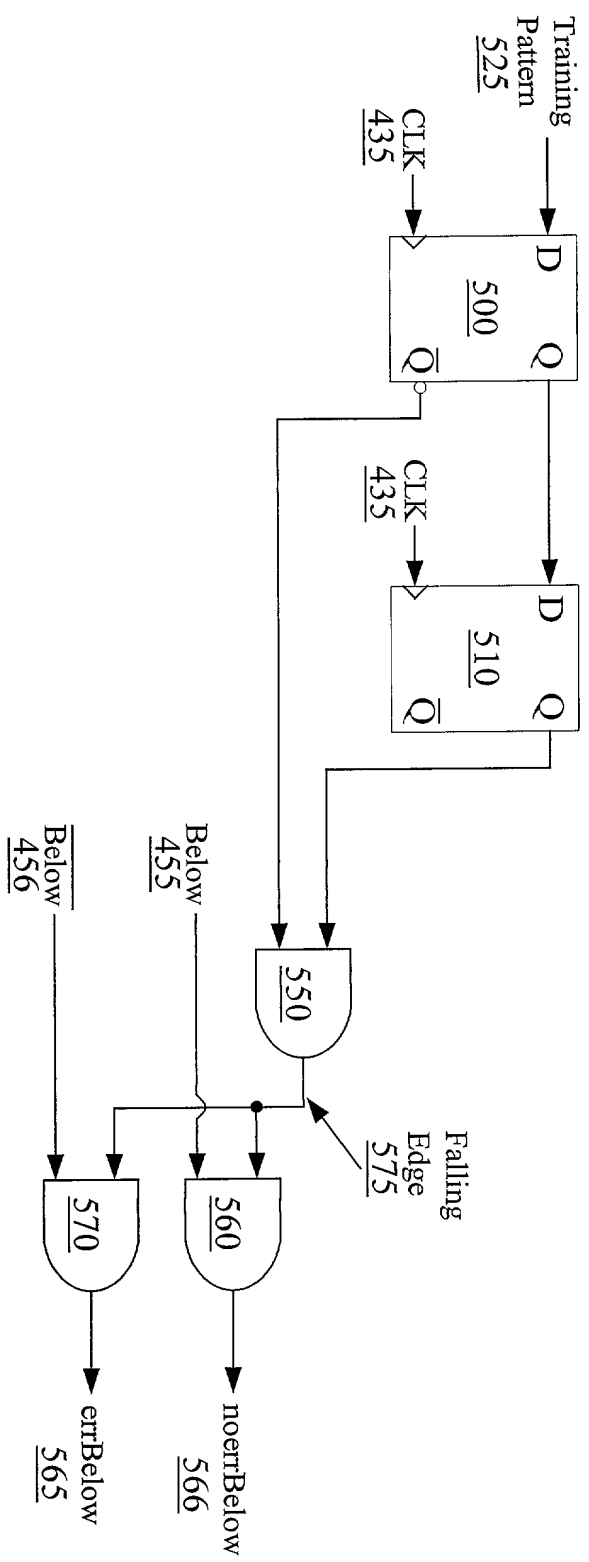
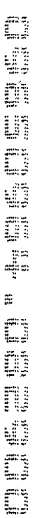


FIG. 4





[illegible]

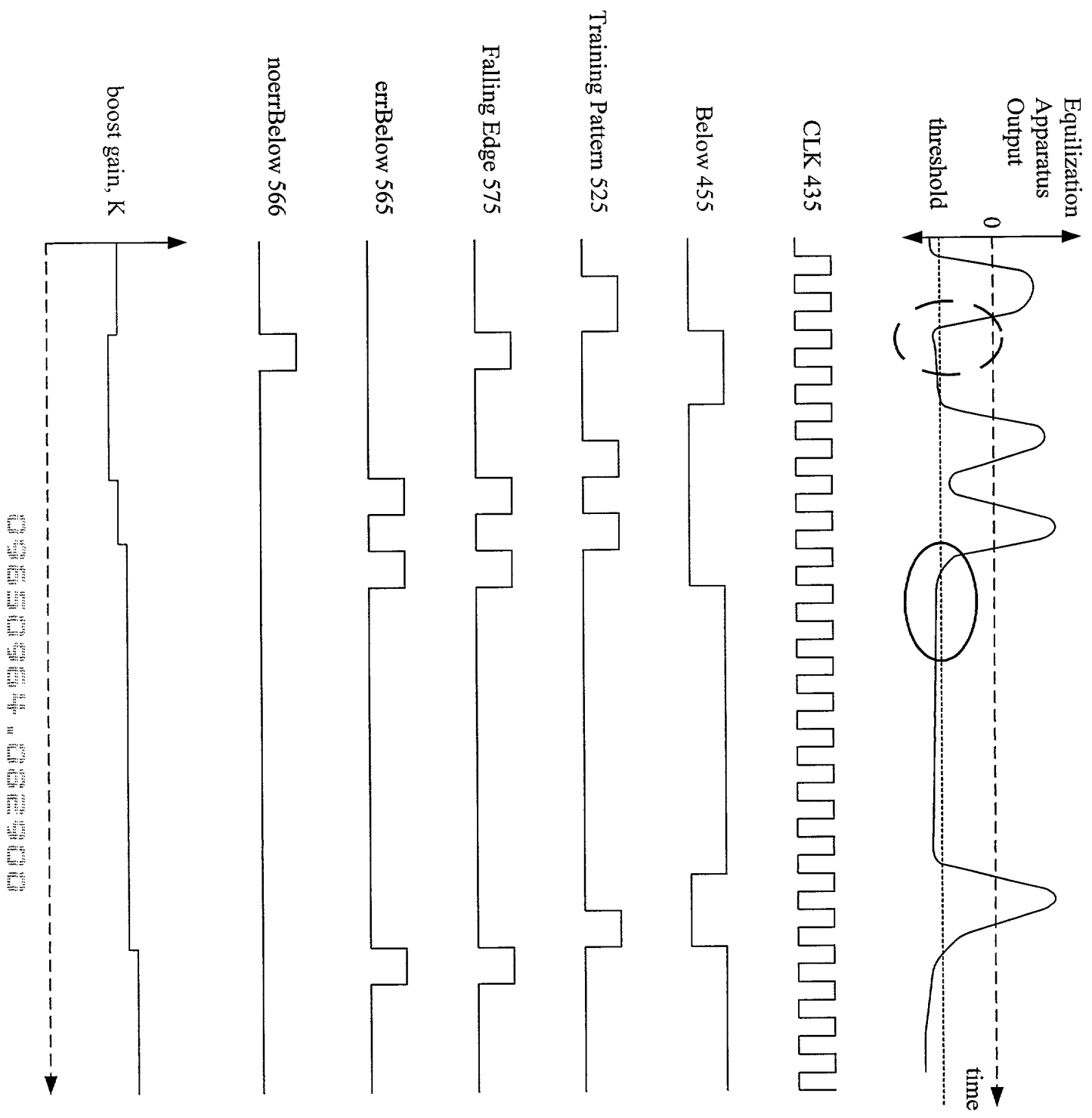


FIG. 7

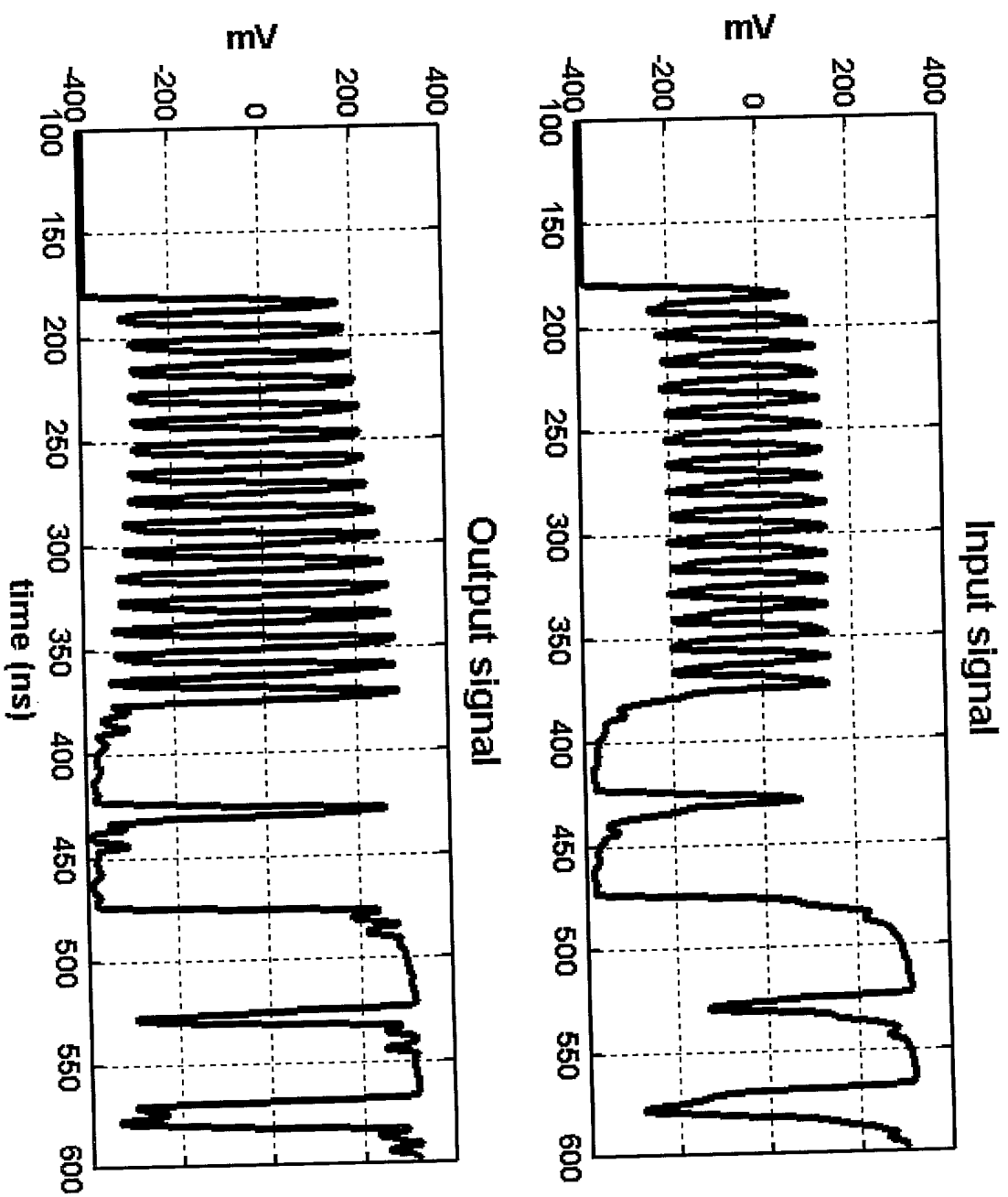


FIG. 8

09690964.000000

## DECLARATION FOR PATENT APPLICATION

As a below named inventor, we hereby declare that:

Our residence, post office address and citizenship are as stated below next to our names.

We believe that we are the original, first and joint inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled **MIXED SIGNAL ADAPTIVE BOOST EQUALIZATION APPARATUS AND METHOD**, the specification of which

  X   is attached hereto.

       was filed on                      as Application Serial No.                     ,  
and was amended by on                     .

We hereby state that we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

We acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

We hereby claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Applications

Priority Claimed

NONE

\_\_\_\_\_

On behalf of Quantum Corporation, Assignee of our entire right, title and interest, we hereby appoint the following attorney(s) and/or agent(s) with full power of substitution to act exclusively for Quantum Corporation to prosecute this application and transact all business in the Patent and Trademark Office connected therewith; JONATHAN B. PENN, Registration No. 32,587, HENRY J. GROTH, Registration No. 39,696. Please address all correspondence and communications to:

HENRY J. GROTH  
Patent Law Manager  
Quantum Corporation  
500 McCarthy Blvd.  
Milpitas, CA 95035  
Telephone (408) 894-5425

All telephone calls should be directed to HENRY J. GROTH, telephone number (408) 894-5425.

Full Name of Inventor: ANDREW BISHOP

Inventor's Signature: \_\_\_\_\_

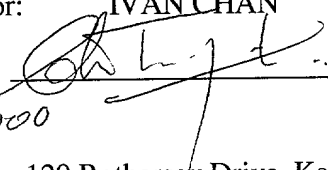
Date: \_\_\_\_\_

Inventor's Residence: 81 Holden Street, Shrewsbury, MA 01545

Citizenship: Canada

Post Office Address: Same as residence address above.

Full Name of Inventor: IVAN CHAN

Inventor's Signature:  \_\_\_\_\_

Date: 26 July 2000

Inventor's Residence: 120 Rothersay Drive, Kanata, Ontario, Canada

Citizenship: Canada

Post Office Address: Same as residence address above.

On behalf of Quantum Corporation, Assignee of our entire right, title and interest, we hereby appoint the following attorney(s) and/or agent(s) with full power of substitution to act exclusively for Quantum Corporation to prosecute this application and transact all business in the Patent and Trademark Office connected therewith; JONATHAN B. PENN, Registration No. 32,587, HENRY J. GROTH, Registration No. 39,696. Please address all correspondence and communications to:

HENRY J. GROTH  
Patent Law Manager  
Quantum Corporation  
500 McCarthy Blvd.  
Milpitas, CA 95035  
Telephone (408) 894-5425

All telephone calls should be directed to HENRY J. GROTH, telephone number (408) 894-5425.

Full Name of Inventor: ANDREW BISHOP

Inventor's Signature: 

Date: June 27, 2000

Inventor's Residence: 81 Holden Street, Shrewsbury, MA 01545

Citizenship: Canada

Post Office Address: Same as residence address above.

Full Name of Inventor: IVAN CHAN

Inventor's Signature: \_\_\_\_\_

Date: \_\_\_\_\_

Inventor's Residence: 120 Rothersay Drive, Kanata, Ontario, Canada

Citizenship: USA

Post Office Address: Same as residence address above.

Full Name of Inventor: RUSSELL W. BROWN

